AF/2815

DOCKET NO. MICHEJDA 4-6 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	John A. Michejda, *et al.*
Serial No.:	09/882,911
Filed:	June 15, 2001
For:	A SEMICONDUCTOR DEVICE HAVING A GHOST SOURCE DRAIN REGION AND A METHOD OF MANUFACTURE THEREFOR
Group No.:	2815
Examiner:	Fenty, Jesse A.

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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August 14, 2003 Elizabeth Schumacher
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Sirs:

APPELLANTS' BRIEF UNDER 37 C.F.R. §1.192

This is an appeal from a Final Rejection dated April 10, 2003, of Claims 1-22. The Appellants submit this Brief in triplicate as required by 37 C.F.R. §1.192(a), with the statutory fee of $ 320.00 as set forth in 37 C.F.R.§1.17(c), and hereby authorize the Commissioner to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 08-2395.

This Brief contains these items under the following headings, and in the order set forth below in accordance with 37 C.F.R. §1.192(c):

I. REAL PARTY IN INTEREST

II. RELATED APPEALS AND INTERFERENCES

III. STATUS OF CLAIMS

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X. APPENDIX A - CLAIMS

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Agere Systems, Inc.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1-22 are currently pending in this Appeal.

IV. STATUS OF THE AMENDMENTS

The Examiner mailed a Final Office Action on April 10, 2003, rejecting Claims 1-22. In response, the Appellants filed a Request For Reconsideration on June 9, 2003. The Examiner mailed an Advisory Action on June 20, 2003, indicating that the arguments of the Request for Reconsideration did not place the Application in condition for allowance. The Appellants then filed a Notice of Appeal on June 26, 2003. Accordingly, no amendments were proposed after the latest Final Rejection.

V. SUMMARY OF THE INVENTION

The present invention is directed to a semiconductor device and a method of manufacture therefor. (Summary) As shown in Illustration 1 below (FIGURE 1A of the Patent), the semiconductor device 100, among other things, may include a channel region 130 located in a semiconductor substrate 110 and a trench 140, 145 located adjacent a side of the channel region 130. The semiconductor device 100 further includes an isolation structure 150 located in the trench 140, 145, and a source/drain region 178 located over the isolation structure 150. Located over at least one sidewall of the trench 140, 145, in the embodiment of Illustration 1, is a sidewall spacer 165. (Application: page 10, paragraph 32 thru page 13, paragraph 38; Claims 1, 9 and 17).

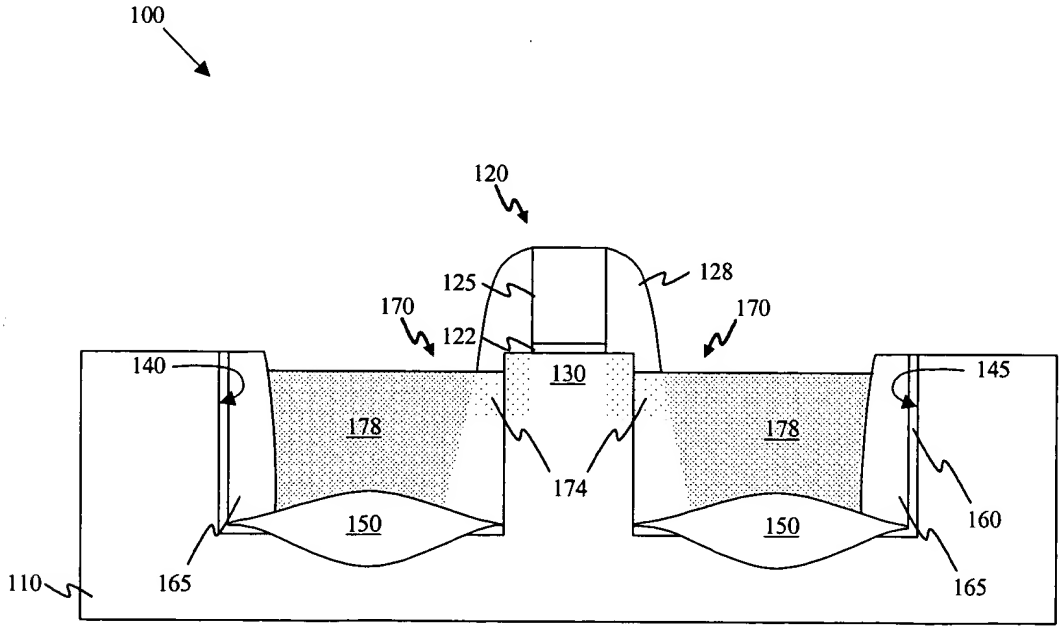

FIGURE 1A

Illustration 1

VI. ISSUES

A. Whether Claims 1, 2, 4, 6, 7, 9, 12, 14, 15, 21 and 22, as rejected by the Examiner, are anticipated under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent No. 6,346,729 to Liang, *et al.* (Liang).

B. Whether Claims 5 and 15, as rejected by the Examiner, are patentably nonobvious in accordance with 35 U.S.C. §103(a) over Liang as applied to Claims 1 and 9, and further in view of U.S. Patent No. 6,287,925 B1 to Yu (Yu).

C. Whether Claims 8 and 16, as rejected by the Examiner, are patentably nonobvious in accordance with 35 U.S.C. §103(a) over Liang.

D. Whether Claims 1, 3, 9, 11, and 17-20, as rejected by the Examiner, are patentably nonobvious in accordance with 35 U.S.C. §103(a) over Liang in view of U.S. Patent No. 5,086,322 to Ishii, *et al.* (Ishii).

VII. GROUPING OF THE CLAIMS

Claims 1-22 stand or fall together.

VIII. SUMMARY OF REFERENCE RELIED ON BY THE EXAMINER

A. Liang

Liang, as shown in Illustration 2 below (FIG. 8 of Liang), is directed to a process for forming a MOSFET device, featuring a heavily doped source/drain region 12, isolated from a semiconductor substrate 1, via use of a thin silicon oxide layer 9. Liang teaches that after formation of a lightly doped source/drain region 6, an opening is created in the semiconductor substrate 1, in a region between insulator spacers 7, on a gate structure, and insulator filled, shallow trench regions 2, resulting in lightly doped source/drain segments 6, remaining under the masking insulator spacers 7. After a thin silicon oxide layer 9 is formed on the exposed silicon surfaces, in the openings, a silicon deposition, and etch back procedures are performed, partially refilling the openings to a depth that still allows the thin silicon oxide layer 9 to be exposed on the sides of the lightly doped source/drain segment 6. After removal of the exposed portion of the thin silicon oxide layer, and after deposition and etch back of another silicon layer, completely filling the openings, a heavily doped source/drain region 12 is formed in the silicon layers, residing in the openings. Liang further teaches that a gate structure 3, 4, 5 is flanked on both sides by the gate sidewall spacers 7.

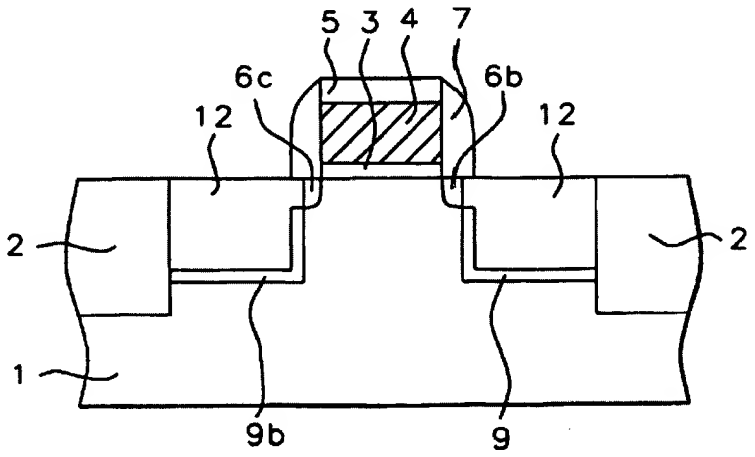

FIG. 8

Illustration 2

B. Yu

Yu is directed to the formation of highly conductive junctions by rapid thermal anneal and laser thermal processes. (Title) Yu, as shown in Illustration 3 below (FIG. 8 of Yu), teaches a MOSFET (Metal Oxide Semiconductor Field Effect Transistor) 200 having a gate structure, including a gate oxide 202, gate electrode and gate silicide 234, flanked on both sides by gate spacers 216. The gate spacers 216 of Yu, as illustrated, are located proximate its channel region. Yu further teaches that a spacer line oxide 218 may interpose the gate structure and the gate spacers 216.

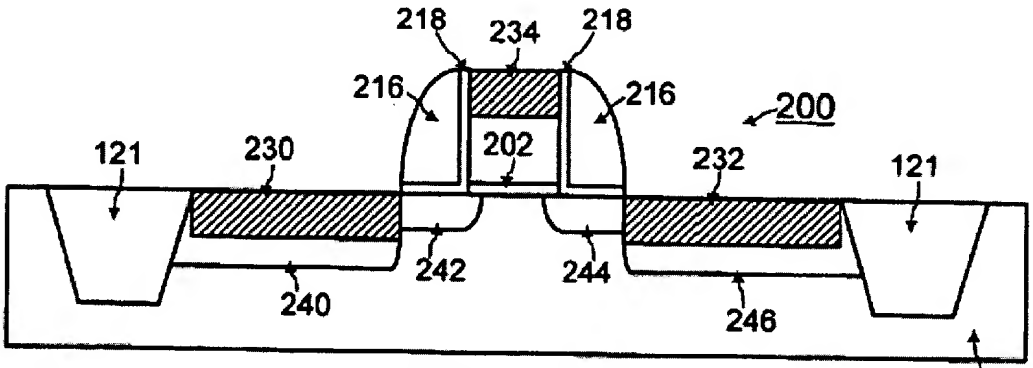

FIG. 8

Illustration 3

C. Ishii

Ishii is directed to an input protection circuit and output driver circuit comprising a MIS transistor device. (Title) Ishii, as shown in Illustration 4 below, teaches a MIS transistor comprising first and second concave grooves 17 opposing to each other with a gate electrode 4 provided therebetween. Ishii further teaches that source and drain regions 8a, 8b are formed on sidewalls of

the concave grooves 17. A configuration of the sidewall surface of the concave groove is selected such that a current density of a punch through current between the source and drain regions becomes uniform. Ishii also teaches forming dielectric layers 15, 16, over the MIS transistor.

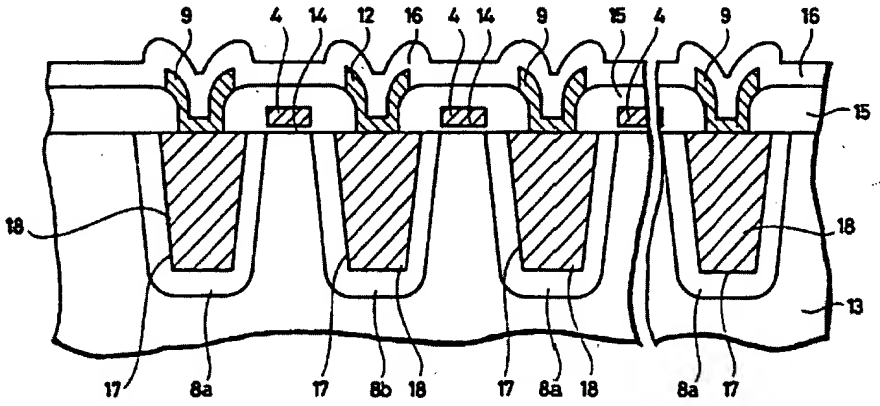

Illustration 4

IX. THE APPELLANTS' ARGUMENTS

The inventions set forth in independent Claims 1, 9 and 17, and their respective dependent claims, are neither anticipated by or made obvious from the references on which the Examiner relies.

A. Rejection of Claims 1, 2, 4, 6, 7, 9, 12, 14, 15, 21 and 22 under 35 U.S.C. §102(e)

Liang fails to anticipate independent Claims 1, 9 and 17, and their dependent claims, because Liang fails to disclose every element of independent Claims 1, 9 and 17. Specifically, Liang fails to disclose the claimed element that a sidewall spacer is located over at least one sidewall of the trench distal the channel region.

In contrast to that presently claimed, Liang specifically discloses that its silicon dioxide layers 9 and 9' are positioned in a base of its trench 8a and along a sidewall contiguous (i.e., proximate) with the channel region. More specifically, independent Claim 1 of Liang requires that "an L shaped, thin silicon oxide layer, comprised of a vertical shape, extending vertically downward from the bottom of said lightly doped source/drain segment [i.e., contiguous with the channel region] and a horizontal shape, extending horizontally from the bottom of said vertical shape of said L shaped thin silicon oxide layer, to the side of an insulator filled shallow trench isolation region." (Claim 1--Emphasis added) While Liang may teach silicon dioxide layers 9 and 9' positioned in a base of its trench 8a and along a sidewall contiguous with the channel region, it does not teach forming a sidewall spacer over at least one sidewall of the trench distal the channel region.

The Examiner asserts a number of things. First, the Examiner asserts that the claim language "a sidewall spacer" is being interpreted very broadly, and thus, the claimed language is being compared to a gate sidewall spacer. Notwithstanding the Examiner's broad interpretation of the claim language "a sidewall spacer," the gate sidewall spacer of Liang is not even located over a sidewall of the trench located distal the channel region. In actuality, the gate sidewall spacer of Liang is located over a sidewall of the trench proximate the channel region.

Second, the Examiner asserts that the term "located over" is interpreted to mean a height differential, rather than one layer covering another, and thus the gate sidewall spacer of Liang is located "over" the distal trench sidewall. It is a well-known principle in patent law that the words of claims must be interpreted in their ordinary meaning unless defined otherwise within the specification. (MPEP 2111.01). Unfortunately, many words in American English, as in other languages, often have multiple meanings. Thus, when an ordinary word in a claim has two or more ordinary meanings, the courts *and* the Examiner should look to the context of the specification to differentiate and to understand what was meant in that particular use. It is clear when FIGUREs 1A-1B and 9-20 and their associated text are taken together in context, that the use of the word "over" is in the sense of "physically over" rather than higher than, as argued by the Examiner. When interpreting a claim, it makes no sense to interpret a word within the claim in any way other than the meaning imparted by the context of the specification. Therefore, the Appellants firmly believe that the Examiner is not at liberty to arbitrarily select an alternative meaning of a word that suits the Examiner's purpose to defeat a claim.

Lastly, the Examiner argues that the phrase "distal the channel region" without any other reference to a distance relationship in a claim is a relative term. Therefore, the Examiner argues that the gate sidewall spacer of Liang is located over a sidewall of the trench distal the channel region. The Examiner is correct when stating that the term distal is a relative term, however, the Examiner is incorrect in arguing that no relationship has been created by the claims. The term distal (or far) is relative to something that is proximate (or near). Thus, when referring to the sidewalls of a trench and saying that one sidewall is distal the channel region, it is relative to the other sidewall that is proximate the channel region. Therefore, as is the case in the claimed invention and Liang, the

trenches have sidewalls that are proximate the channel region and distal the channel region. Unfortunately for the Examiner, the present invention claims that the sidewall spacer is located over the sidewall distal the channel region and Liang discloses that its gate sidewall spacer is located over the sidewall proximate the channel region. These are entirely different teachings.

For the reasons stated above, Liang does not disclose each and every element of the claimed invention and as such, is not an anticipating reference. Because Claims 2, 4, 6, 7, 12, 14, 15, 21 and 22 are dependent upon Claims 1, 9 and 17, Liang also cannot be an anticipating reference for Claims 2, 4, 6, 7, 12, 14, 15, 21 and 22.

B. Rejection of Claims 5 and 15 under 35 U.S.C. §103

The combination of Liang and Yu fails to render obvious the elements of independent Claims 1, 9 and 17, and their dependent claims, because the combination fails to teach or suggest every element of independent Claims 1, 9 and 17. Specifically, the combination fails to teach or suggest the claimed element that a sidewall spacer is located over at least one sidewall of the trench distal the channel region.

The Appellants established above that Liang fails to teach the aforementioned element. Liang also fails to suggest such an element because Liang uses its shallow trench isolation structures 2 to provide its isolation distal the channel region, and therefore would not require a sidewall spacer be located there also. One skilled in the art would not be motivated to take the thin silicon dioxide layers 9, 9b taught by Liang and place it on the sidewall distal the channel without using the present invention as a blueprint. Similarly, one skilled in the art would not be motivated to take the gate

sidewall spacer 7 of Liang and place it over at least one sidewall of the trench distal the channel region. Thus, Liang also fails to teach or suggest such an element.

Similar to Liang, Lu fails to teach or suggest the aforementioned claimed element. The Examiner is using Lu for the sole proposition that an oxide layer may be located between the sidewall spacer and the at least one sidewall of the trench. Notwithstanding the merits of the Examiner's position, Lu also fails to teach or suggest the element that a sidewall spacer is located over at least one sidewall of the trench distal the channel region. A teaching or suggestion of placing an oxide layer between the sidewall spacer and the at least one sidewall of the trench is dissimilar to a teaching that a sidewall spacer be located over at least one sidewall of the trench distal the channel region, as required by independent Claims 1, 9 and 17.

Thus, Liang, individually or in combination with Yu fails to teach or suggest the invention recited in independent Claims 1 and 9. Because Claims 5 and 15 are dependent upon Claims 1 and 9, the combination also does not render obvious Claims 5 and 15. Claims 5 and 15 are therefore not obvious in view of Liang and Yu.

C. Rejection of Claims 8 and 16 under 35 U.S.C. §103

For the reasons set forth above, Liang fails to render obvious the elements of independent Claims 1, 9 and 17. Claims 8 and 16 currently depend from independent Claims 1 and 9, respectively, thus Liang fails to teach or suggest all of the elements currently included within dependent Claims 8 and 16.

D. Rejection of Claims 1, 3, 9, 11, and 17-20 under 35 U.S.C. §103

The Appellants established in the §103 rejection above that Liang fails to teach or suggest the element that a sidewall spacer is located over at least one sidewall of the trench distal the channel region, as required by independent Claims 1, 9 and 17. Ishii also fails to teach or suggest this element, and therefore fails to correct the deficiencies of Liang.

The Examiner is using Ishii for the sole proposition that dielectric layers are located over the semiconductor devices and have interconnect structures located therein. Notwithstanding the merits of the Examiner's position, Ishii also fails to teach or suggest the element that a sidewall spacer be located over at least one sidewall of the trench distal the channel region. A teaching or suggestion of dielectric layers located over the semiconductor devices having interconnect structures located therein, is dissimilar to a teaching that a sidewall spacer is located over at least one sidewall of the trench distal the channel region, as required by independent Claims 1, 9 and 17.

Thus, Liang, individually or in combination with Ishii fails to teach or suggest the invention recited in independent Claims 1, 9 and 17. Because Claims 3, 11, and 18-20 are dependent upon Claims 1, 9 and 17, the combination also does not render obvious Claims 3, 11, and 18-20. Claims 1, 3, 9, 11, and 17-20 are therefore not obvious in view of Liang and Ishii.

For the reasons set forth above, the Claims on appeal are not anticipated by Liang. Further, the Claims are patentably nonobvious over Liang in view of Yu and Ishii. Accordingly, the

Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of all of the Appellants' pending claims.

Respectfully submitted,

Hitt Gaines, P.C.

Greg H. Parker
Registration No. 44,995

Dated: 6-14-03

P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800
(972) 480-8865
E-Mail: gparker@abstractassets.com

X. APPENDIX A - CLAIMS

1. A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation structure located in the trench;

a sidewall spacer located over at least one sidewall of the trench distal the channel region; and

a source/drain region located over the isolation structure.

2. The semiconductor device as recited in Claim 1 wherein the trench is a first trench and the semiconductor device further includes a second trench located on an opposing side of the channel region, wherein the isolation structure is a first isolation structure located in the first trench and the semiconductor device further includes a second isolation structure located in the second trench, and wherein the source/drain region is a first source/drain region and the semiconductor device further includes a second source/drain region located over the second isolation structure.

3. The semiconductor device as recited in Claim 1 wherein the source/drain region comprises polysilicon.

4. The semiconductor devices as recited in Claim 1 wherein the source/drain region comprises epitaxial silicon.

5. The semiconductor device as recited in Claim 1 wherein an oxide layer is located between the sidewall spacer and the at least one sidewall of the trench.

6. The semiconductor device as recited in Claim 1 wherein the sidewall spacer comprises a nitrided layer.

7. The semiconductor device as recited in Claim 1 wherein the isolation structure comprises an oxide.

8. The semiconductor device as recited in Claim 1 wherein the source/drain region includes a lightly doped source/drain region having a dopant concentration ranging from about 1E16 atoms/cm^3 to about 1E17 atoms/cm^3, and a source/drain contact region having a dopant concentration up to about 1E22 atoms/cm^3.

9. A method of manufacturing a semiconductor device, comprising:

forming a channel region in a semiconductor substrate;

forming a trench adjacent a side of the channel region;

forming an isolation structure in the trench;

forming a sidewall spacer over at least one sidewall of the trench distal the channel region; and

forming a source/drain region over the isolation structure.

10. The method as recited in Claim 9 wherein forming the trench includes forming a first trench and the method further includes forming a second trench on an opposing side of the channel region, wherein forming the isolation structure includes forming a first isolation structure in the first trench and the method further includes forming a second isolation structure in the second trench, and wherein forming the source/drain region includes forming a first source/drain region and the method further includes forming a second source/drain region over the second isolation structure.

11. The method as recited in Claim 9 wherein forming the source/drain region includes forming a polysilicon source/drain region.

12. The methods as recited in Claim 9 wherein forming the source/drain region includes epitaxially growing the source/drain region from the channel region.

13. The method as recited in Claim 9 further including forming an oxide layer between the sidewall spacer and the at least one sidewall of the trench.

14. The method as recited in Claim wherein forming a sidewall spacer includes forming a nitrided layer.

15. The method as recited in Claim 9 wherein forming an isolation structure includes forming an isolation structure comprising an oxide.

16. The method as recited in Claim 9 wherein forming a source/drain region includes forming a lightly doped source/drain region having a dopant concentration ranging from about 1E16 atoms/cm^3 to about 1E17 atoms/cm^3, and forming a source/drain contact region having a dopant concentration up to about 1E22 atoms/cm^3.

17. An integrated circuit, comprising:

semiconductor devices, including;

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation structure located in the trench;

a sidewall spacer located over at least one sidewall of the trench distal the channel region; and

a source/drain region located over the isolation structure; and

dielectric layers located over the semiconductor devices and having interconnect structures located therein that electrically connect the semiconductor devices to form an operative-integrated circuit.

18. The integrated circuit as recited in Claim 17 wherein the trench is a first trench and the semiconductor device further includes a second trench located on an opposing side of the channel region, wherein the isolation structure is a first isolation structure located in the first trench and the semiconductor device further includes a second isolation structure located in the second trench, and

wherein the source/drain region is a first source/drain region and the semiconductor device further includes a second source/drain region located over the second isolation structure.

19. The integrated circuit as recited in Claim 17 wherein the isolation structure comprises an oxide.

20. The integrated circuit as recited in Claim 17 wherein the semiconductor devices form part of an N-type metal oxide semiconductor (NMOS) device, a P-type metal oxide semiconductor (PMOS) device, a complementary metal oxide semiconductor (CMOS) device, a bipolar device, or a memory device.

21. The semiconductor device as recited in Claim 1 wherein the sidewall spacer is not contiguous the side of the channel region.

22. The method as recited in Claim 9 wherein the sidewall spacer is not formed contiguous the side of the channel region.